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Technical Datasheet

takeMS BD512TEC413

Description

These Memory devices are JEDEC standard unbuffered DIMM modules, based on CMOS DDR SDRAM technology.
These devices consist of CMOS DDR SDRAMs in TSOP packages on a 184-pin glass epoxy substrate.The memory array is designed with Double Data Rate (DDR) Synchronous DRAMs for unbuffered applications.
Decoupling capacitors are mounted on the PCB board in parallel for each DDR SDRAM, which provides proper voltage supply impedance over the whole frequency range of operations, in accordance with JEDEC specifications. These modules feature Serial Presence Detect (SPD) based on a serial EEPROM device.

Features
JEDEC Standard 184-pin small outline, dual in-line memory module
2.5V±0.1V VDD and VDDQ Power supply
All inputs and outputs are compatible with SSTL_2 interface
Fully differential clock operations
DLL aligns DQ and DQS transition with CK transition
Serial Presence Detect (SPD) with EEPROM
Module layout is based on JEDEC standard routing guidelines
Programmable Burst Length 2 / 4 / 8 with both sequential and interleave mode
JEDEC standard form factor
Edge-aligned DQS with data outs and Center-aligned DQS with data inputs
Auto refresh and self refresh supported
Operating Temperature 0°C ~ 75°C

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Technical details

- **512 MB logdimm module**
- **64Mx8 IC organisation**
- **x64 module organisation**
- **333 MHz / PC 2700**
- **single sided / 8 ICs**
- **CAS Latency 2,5 at max. memclock**

For pin configuration please check www.takems.com/support/index.php

If you have any questions regarding our products you can contact us via email: info@takems.com

Order-No.: **BD512TEC413**

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